Switch-Debouncer IC Creates A Long-Period Timer

This application depicts how to reduce power in systems that only require the µP to be used periodically. By using a debounce IC circuit, the µP can be set to monitor over long timer periods, thus allowing it to enter low-power mode for the remaining time. As a result, overall power is reduced.

One major application for long-period timers is in remote weather-data stations. These stations measure environmental conditions at regular time intervals and transmit the results to a central collecting facility. Since these small weather stations are often located in remote areas that depend on solar-cell power during cloudy weather, power efficiency is an important factor in their design. Size and cost are also prominent considerations.

A minimum-component configuration is possible for an all-surface-mount, low-power, long-period timer. This design can be implemented with two low-cost components and firmware that reduces power consumption by allowing the microcontroller (uC) to enter a "sleep mode." Later, the µC is awakened to perform regulary scheduled measurements. The circuit shown in Figure 1 accomplishes this task by taking advantage of the extra section in a dual CMOS switch debouncer (U1).

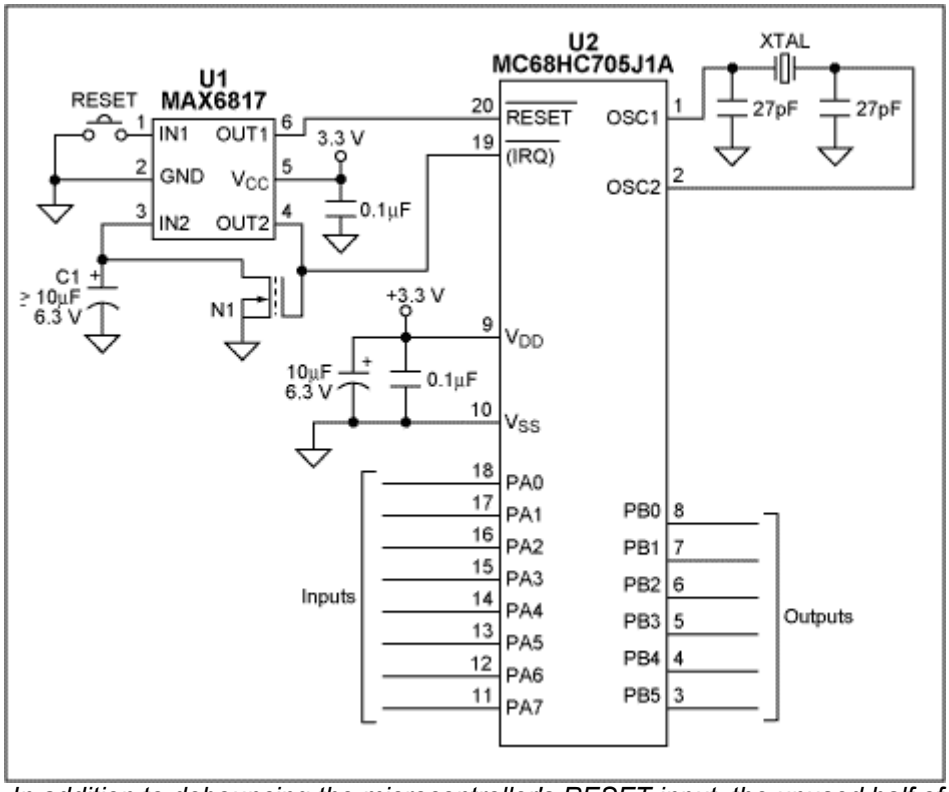

Figure 1. In addition to debouncing the microcontroller's RESET input, the unused half of this dual switch-debouncer IC (U1) is used to implement a long-period timer function.

The µC (U2) provides 32 bytes of RAM and 1232 bytes of EPROM. (A low-cost, one-time programmable version is also available.) The IN1/OUT1 pins of the dual debouncer U1 are configured to debounce the µC's system-reset pulse. The IN2/OUT2 pair is configured as the long-period timer. Capacitor C1 and a 63kΩ (typical) pull-up resistor internal to U1 form the time constant for this purpose.

U1 initiates a 50ms delay when the C1 voltage reaches U1's input-voltage threshold. Following this delay, OUT2 turns on the n-channel digital FET N1, which must remain on long enough to completely discharge C1 in preparation for the next timing cycle. The second transition (high-to-low) at IN2 initiates another 50ms delay. Following this delay, the cycle repeats. Thus, the timer period can be calculated using the following equation:

$$\text{Period (s)} = (63k \cdot C1 \cdot (-\ln(1 - V_T/V_{CC})) + 0.1s)$$

Table 1 shows the input threshold voltage (V_T) for U1 at various operating voltages (V_{CC}).

Table 1

Threshold versus V_{CC} Voltage For MAX6817 Switch Debouncer	
Table System Voltage, V_{CC}	Table Threshold Voltage, V_T
2.7V	1.30V
3.0V	1.45V
3.3V	1.50V
5.0V	2.00V

The following equation can be used to determine the C1 value for a desired timer period:

$$C1 = (\text{Period} - 0.1s)/(63k \cdot (-\ln(1 - V_T/V_{CC})))$$

where Period equals the desired time delay in seconds.

Remote weather stations report at certain intervals, and the time of these reports is recorded by the collection station. Since timing is not critical, the C1 capacitor can be a tantalum type with ±20% tolerance. If tighter timing is desired, a surface-mount ceramic capacitor can be substituted for C1.

The digital FET N1 was chosen for its low-level gate drive, which enables it to operate properly in 3 to 5V circuits. If a different FET is substituted, it must be capable of discharging C1 completely before U1 changes the output state to low. Specifically, it should provide a discharge time ($5R_{DSON}C1$) less than 50ms. If the shortest possible period is desired, U1 can be configured as a 10Hz stable multivibrator by removing C1 (leaving the drain of N1 connected to pin 3 of U1).

The program code, written in 68HC705 assembler, for the long-period timer is available for download at the Maxim Software Page.

A similar version of this article appeared in the October 1, 2001 issue of *Electronic Design* magazine.

DI446, December 2001

MORE INFORMATION

MAX6817: QuickView -- Full (PDF) Data Sheet (200k) -- Free Sample